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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/467,992 | 12/20/1999 | LEONARD FORBES | 303.389US2 | 3099 |

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EXAMINER

LEE, EUGENE

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2815

DATE MAILED: 05/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/467,992

Applicant(s)

FORBES ET AL.

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-19, 22, 23, 25-27, 29 and 31-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 17-19, 22, 23, 25-27, 29 and 31-51 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 December 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the trench capacitor formed in a trench and **coupled to the first source/drain region** must be shown or the feature(s) canceled from the claim(s). In FIG. 1, first source/drain 106 is isolated from the trench capacitor by a body region 108 and there is no coupling. In FIG. 6, the second source/drain 608 is coupled to the trench capacitor, not the first source/drain 604. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 17 thru 21, 22, 23, 25 thru 27, 29, and 31 thru 50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 17, it is unclear how the second plate 120 would be “integral” with first source/drain region 106. The second plate 120 and the first source/drain region 106 are completely separated from each other, as shown in FIG. 1 of applicant’s drawings. In FIG. 6, the second plate 624 does not appear “integral” with first source 604.

It is still unclear how the applicant is defining the word "integral". The Office does not know whether to define the word "integral" as meaning "connected to", "the same structure", "being on top", etc. On page 4, paragraph 3 of applicant's amendment filed 2/12/02, the applicant states that the "first plate and second plate integral with the first source region of the transistor." The Office does not understand how the first plate and second plate could be integral with the first source region of the transistor. In FIG. 1, the second plate 120 is isolated from first source/drain region 106 and in FIG. 6 the second plate 624 is isolated from first source/drain region 604.

In claim 22, the applicant states "the first source/drain includes integral therewith a first polycrystalline plate", however, the first source/drain 106 is not "integral" with a first polycrystalline plate 110. In this case, it is not clear whether "integral" means "above" or "part of the same structure" as stated on page 6, paragraph 5 of applicant's amendment filed 2/12/02.

In claim 26, the applicant states "a first plate of the trench capacitor is integral with a first source/drain region." See paragraph above.

The rest of independent claims 31, 33, 34, 35, and 41 contain this ambiguity and the applicant is required to clarify.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Insofar as definite, claims 17 thru 19, 22, 23, 26, 27, 29, 31 thru 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wen '509. For example, in FIG. 3, Wen discloses a memory cell trench storage capacitor 100 comprising a polysilicon layer (second plate) 114, capacitor dielectric layer (insulator layer) 116, doped polysilicon fill (first plate) 118 and p+ doped semiconductor substrate 110.

Regarding the above claims, it is well known in the art that capacitor plates are inherently connected to source/drain regions of peripheral transistors. It is also well known that bit and word lines are coupled to source/drain regions and gates of access transistors along with a column decoder and row decoder to access the cells of an array. These positions are supported by Pfiester '385, Forbes et al. '618, and Wahlstrom '452.

The basis of the combination is that Wen's trench capacitor is used in conventional memory cells, for example, like the ones shown in Pfiester '385, Forbes et al. '618 and Wahlstrom '452. It would have been obvious to one of ordinary skill in the art at the time of invention to use the trench capacitor of Wen in typical memory cells like Pfiester, Forbes and Wahlstrom since Wen specifically states that the trench capacitor is used for memory cells and, therefore, can provide a capacitor with increased surface area and capacitance for the memory cell (as stated in the abstract) to offset the continued miniaturization of semiconductor devices.

6. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester '385 in view of Wen '509. Pfiester discloses (see, for example, FIG. 1) a memory cell comprising a lateral transistor 56, source/drain regions 54, semiconductor material layer (body region) 32, trench capacitor 50, substrate (first plate) 34, capacitor plate (second plate) 66, and dielectric layer 60. A contact from the capacitor plate extends to the source/drain region. Pfiester does not

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disclose a micro-roughened polysilicon surface. However, Wen teaches a trench capacitor wherein a textured polysilicon layer 118 resides on the inner surface of the substrate 110. Wen teaches (see, for example, column 3, lines 25-28) that the textured polysilicon layer increases the area of the capacitor and therefore increases its capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the textured polysilicon layer in Pfister's invention in order to increase the capacitance.

Response to Arguments

7. Applicant's arguments filed 2/11/02 have been fully considered but they are not persuasive. Please see rejection above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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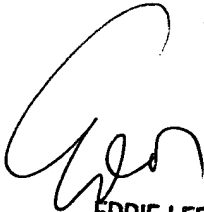
INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
May 2, 2002



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800